DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ronal J. Ward on March 22nd 2010.

The application has been amended as follows:

1. **(Currently Amended)** A circuit for multiplexing a plurality of data signals into an output data stream comprising:

a plurality of circuit elements, wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal received from a source other than one of the plurality of circuit elements, wherein an output of each circuit element of said plurality of circuit elements comprises an individual data signal of said plurality of data signals and wherein said first clock signal is ~~substantially~~ in-phase with said transition; [[and]]

a selector coupled to said plurality of circuit elements for receiving each of the individual output data signals from the plurality of circuit elements and for sequentially selecting each of said individual data signals to generate said output data stream as

the output of the selector, wherein said selector is clocked to control said selecting by a second clock signal received from a source other than one of the plurality of circuit elements, wherein said second clock signal is out of phase with respect to said first clock signal by a fixed offset; and

a compensator that is separate from the plurality of circuit elements coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit elements, wherein said second clock signal is transmitted to said selector through said compensator, and wherein said compensator retards said second clock signal to said selector by a compensating delay corresponding to said clock-to-data delay.

2. **(Original)** The circuit as recited in Claim 1 wherein said fixed offset comprises a quadrature offset.

3. **(Original)** The circuit as recited in Claim 1 wherein said fixed offset comprises a delay.

4. **(Original)** The circuit as recited in Claim 3 wherein said delay comprises a quadrature delay.

5. **(Original)** The circuit as recited in Claim 1 further comprising a clock generator coupled to said selector for generating said fixed offset.

6. **(Original)** The circuit as recited in Claim 5 wherein said clock generator comprises a coupled oscillator circuit.

7. **(Original)** The circuit as recited in Claim 5 wherein said clock generator comprises a divide-by-two circuit.

8. **(Original)** The circuit as recited in Claim 3 wherein said delay comprises a propagation delay.

9. **(Original)** The circuit as recited in Claim 8 further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.

10-12. **(Cancelled)**

13. **(Original)** The circuit as recited in Claim 1 wherein a part of said plurality of circuit elements comprises a flip-flop.

14. **(Currently Amended)** In a circuit comprising a plurality of circuit elements each for providing a data signal with transitions in response to a clock signal and a selector coupled to said plurality of circuit elements for selecting said data signals for an output data stream, a method for multiplexing a plurality of said data signals into an output data stream comprising:

providing first and second clock signals received from a source other than one of the plurality of circuit elements, wherein said second clock signal is out-of-phase with respect to said first clock signal by a fixed offset;

clocking said circuit elements with said first clock signal to control said transitions of said data signal; [[and]]

clocking said selector with said second clock to sequentially select a plurality of said data signals that are received as input for the selector for said output data stream and wherein said second clock is received as a separate input from the plurality of said data signals; and

delaying said second clock signal by a compensating delay corresponding to a delay from said first clock signal to said transitions of said circuit elements.

15. **(Original)** The method as recited in Claim 14 wherein said fixed offset comprises a quadrature offset.

16. **(Original)** The method as recited in Claim 14 wherein said fixed offset comprises a delay.

17. **(Original)** The method as recited in Claim 16 wherein said delay comprises a quadrature delay.

18. **(Original)** The method as recited in Claim 16 wherein said delay is generated by a clock generator coupled to said selector.

19. **(Original)** The method as recited in Claim 18 wherein said clock generator comprises a coupled oscillator circuit.

20. **(Original)** The method as recited in Claim 18 wherein said clock generator comprises a divide-by-two circuit.

21. **(Original)** The method as recited in Claim 16 wherein said delay comprises a propagation delay.

22. **(Original)** The method as recited in Claim 21 further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.

23. **(Cancelled)**

24. **(Cancelled)**

25. **(Currently Amended)** A system for multiplexing a plurality of data signals into an output data stream comprising:

a plurality of circuit elements, wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal received from a source other than one of the plurality of circuit elements, wherein an output of each circuit element of said plurality of circuit elements comprises an individual

data signal of said plurality of data signals and wherein said first clock signal is ~~substantially~~ in-phase with said transition;

a selector coupled to said plurality of circuit elements for receiving each of the individual output data signals from the plurality of circuit elements and for sequentially selecting each of said individual data signals to generate said output data stream as the output of the selector, wherein said selector is clocked to control said selecting by a second clock signal received from a source other than one of the plurality of circuit elements, wherein said second clock signal is out of phase with respect to said first clock signal by a fixed quadrature delay; and

a compensator that is separate from the plurality of circuit elements coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit elements, ~~element,~~ wherein said second clock signal is transmitted to said selector through said compensator, and wherein said compensator retards said second clock signal to said selector by a compensating delay corresponding to said clock-to-data delay.

26. **(Original)** The system as recited in Claim 25 further comprising a clock generator coupled to said selector for generating said fixed quadrature delay.

27. **(Original)** The system as recited in Claim 26 wherein said clock generator comprises a circuit selected from the group consisting essentially of a coupled oscillator circuit and a divide-by-two circuit.

28. **(Original)** The system as recited in Claim 26 wherein said quadrature delay comprises a propagation delay.

29. **(Original)** The system as recited in Claim 28 wherein said clock generator comprises a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.

30. **(Original)** The system as recited in Claim 25 wherein a part of said plurality of circuit elements comprises a flip-flop.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DADY CHERY whose telephone number is (571)270-1207. The examiner can normally be reached on Monday - Thursday 8 am - 4 pm ESt.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. VU can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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